B.Sc. 3rd Semester (Honours) Examination, 2019-20
ELECTRONICS

Course ID : 31712 **Course Code : SHELC-302C-6(T)**

Course Title: Digital Electronics and Verilog (VHDL)

Time: 1 Hour 15 Minutes **Full Marks: 25**

The figures in the right hand side margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

1. Answer *any three* of the following questions: 1×3=3

(a) Using 2's complement method subtract 1010_2 from 1101_2.

(b) Convert the given hexadecimal number $(23A)_{16}$ to binary number.

(c) Find the decimal equivalent of the binary number 1010111 and 001011.

(d) Represent-14 in 1's complement form.

(e) What is a demultiplexer?

2. Answer *any three* of the following questions: 2×3=6

(a) Draw the symbol of an X-NOR gate and give its truth table.

(b) A Boolean expression is given as $Y = (A + B)(\bar{A} + \bar{B})$. Prove that this logic diagram is equivalent to an EX-OR gate.

(c) Prove the Boolean identity $AB + \bar{A}\bar{B} = \overline{A\bar{B} + \bar{A}B}$.

(d) What is a decode counter?

(e) What are ripple counters?

(f) Write down the exitation table of S-R and J-K flip-flops.

3. Answer *any two* of the following questions: 5×2=10

(a) What is a Multiplexor? Explain the function of 8:1 MUX and design the same using different logic gates.

(b) What is a half-adder? Why is it so called? Design a half-adder by using Universal logic gates.

(c) Simplify the following Boolean function using Karrnaugh mapping and draw the logical diagram using NAND gates only. $F(A, B, C, D) = \sum_m(0,1,2,4,7,8,9,12,13)$

(d) Write down the truth-table of half-subtractor. Design the same using NAND gates only.

4. Answer *any one* question: 6×1=6

    (a) Describe the operation of a 4 bit ripple counter using 4JK flip-flops. Draw the proper input output waveforms of the counter.

    (b) What is the need of clocking a flip-flop? Give the truth-table of a clocked SR flip-flop constructed with NAND gates and explain the operation of it.

    (c) Draw the basic circuit diagram of TTL NAND gate and explain its operation.

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